UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/622,863 | 07/18/2003 | Horng-Huei Tseng | | 2915 |

23616 7590 08/12/2005

LAW OFFICES OF CLEMENT CHENG
17220 NEWHOPE STREET #127
FOUNTAIN VALLEY, CA 92708

| EXAMINER | |
|---|---|
| VINH, LAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 1765 | |

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/622,863 | TSENG, HORNG-HUEI | |
| | Examiner | Art Unit | |
| | Lan Vinh | 1765 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsieh (US 6,326,263)

Hsieh discloses a method for manufacturing a flash memory cell on a substrate, the method comprising the steps of:

forming a tunneling dielectric layer 54/oxide on the substrate 52 (col 3, lines 45-47)

forming a first conductive layer 56/polysilicon on the tunneling dielectric layer 54 (col 3, lines 53-54)

patterning the polysilicon layer 56, the tunneling dielectric 54 to form trenches in the substrate (col 3, lines 51-54; fig. 9)

depositing a gap-filling material 62 into said trenches over the substrate (col 4, lines 6-7; fig. 9)

removing a portion of said gap-filling material to form trench isolations pattern 64 and self-aligned portion of a floating gate adjacent to the trench isolations, etching a

portion of said trench isolations to form slots between the etched conductive layer 56/first conductive layer (col 4, lines 8-15; fig. 10)

forming a polysilicon layer 66/second conductive layer over a surface of the slots and the etched first conductive layer 56 (col 4, lines 26-28; fig. 11)

etching the second conductive layer 66 , thereby forming sidewall spacers 68 on the slot (col 4, lines 35-37; fig. 12)

forming a dielectric layer 72/second dielectric on the trench isolation, the sidewall spacers and the conductive layer 56 (col 4, lines 44-45; fig. 13 )

forming a patterned conductive control gate layer 74/doped polysilicon on the second dielectric layer 72 (col 4, lines 46-47; fig. 13)

The limitations of claims 3, 6 have been discussed above

Regarding claims 4-5, Hsieh discloses forming a dielectric layer 72 of ONO dielectric (col 4, lines 44-45)

3. Claims 7-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsieh (US 6,326,263)

Hsieh discloses a method for manufacturing a flash memory cell on a substrate, the method comprising the steps of:

forming a tunneling dielectric layer 54/oxide on the substrate 52 (col 3, lines 45-47)

forming a first conductive layer 56/polysilicon on the tunneling dielectric layer 54 (col 3, lines 53-54)

patterning the polysilicon layer 56, the tunneling dielectric 54 to form trenches in the substrate (col 3, lines 51-54; fig. 9)

depositing a gap-filling material 62 into said trenches over the substrate (col 4, lines 6-7; fig. 9)

removing a portion of said gap-filling material to form trench isolations pattern 64 and self-aligned portion of a floating gate adjacent to said trench isolations, etching a portion of said trench isolations to form slots between the etched conductive layer 56/first conductive layer (col 4, lines 8-15; fig. 10)

forming a dielectric layer 72/second dielectric on the trench isolation, the sidewall spacers and the conductive layer 56 (col 4, lines 44-45; fig. 13 )

forming a patterned conductive control gate layer 74/doped polysilicon on the second dielectric layer 72 (col 4, lines 46-47; fig. 13)

Regarding claim 8, Hsieh discloses the step of forming a polysilicon layer 66/third conductive layer before forming dielectric layer 72 (col 4, lines 26-28; fig. 11), etching the conductive layer 66/third conductive, thereby forming sidewall spacers 68 (col 4, lines 35-37; fig. 12)

The limitations of claims 9, 12 have been discussed above

Regarding claims 10-11, Hsieh discloses forming a dielectric layer 72 of ONO dielectric (col 4, lines 44-45)

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh (US 6,326,263) in view of Lee et al (US 6,380,032)

Hsieh method has been described above. Unlike the instant claimed invention as per claim 2, Hsieh fails to disclose the step of forming a fourth conductive layer before forming the second conductive layer.

Lee discloses a method for forming a flash memory cell comprises the step of the step of forming a polysilicon conductive layer 260/fourth conductive layer before forming the second conductive layer 280 (col 7, lines 13-16; fig. 10A)

Since both Hsieh and Lee are directed to a method of forming a flash memory cell device having a control gate, one skilled in the art at the time the invention was made would have found it obvious to modify Hsieh method by adding the step of forming a

fourth conductive layer before forming the second conductive layer to form a stacked gate pattern and common source line as taught by Lee (col 7, lines 25-31)

***Response to Arguments***

6. Applicant's arguments filed 6/18/2005 have been fully considered but they are not persuasive.

Applicants argue that contrary to the teaching of Hsieh, the claimed invention, as per claim 1, patterns the first conductive layer, the tunneling dielectric layer and the substrate to form trenches therein together without previously patterning the first conductive layer and the tunneling dielectric layer. This argument is unpersuasive for the following reasons: the argument does not commensurate with the scope of claim 1 since claim 1 does not require/recite patterning the first conductive layer, the tunneling dielectric layer and the substrate to form trenches therein together without previously patterning the first conductive layer and the tunneling dielectric layer. In addition since fig. 9 of Hsieh shows the trenches 64, in the substrate 52, are formed by the patterned layers 54/tunneling dielectric layer, 56/first conductive layer, 52/substrate, it reads on the claimed limitation of "patterning said first conductive layer, said tunneling dielectric layer and said substrate to form trenches therein"

Applicants further argue that according to MPEP & 2141.02, the cited reference must be considered in its entirely, thus the sacrificial layer 58 is a crucial element in the method of Hsieh and the omission of the sacrificial layer 58 would violate the intended purpose of the teaching of Hsieh so that Hsieh actually disclose a different method

comparing with the claimed invention. This argument is unpersuasive because although the examiner recognizes that the sacrificial layer 58 is a crucial element in the method of Hsieh, the examiner also notes that the claim language of "comprising", as recited in claim 1, does not limit the claimed invention to the claimed steps or excluding additional steps to be performed. Thus, the examiner asserts that Hsieh method is similar to the claimed method, as recited in claim 1

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Conclusion***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
August 5, 2005